43 copy

Two marks

MAy2016,Dec2016,May 2017,Dec 2015,Dec 2014

Unit-1

1. **What is meant Channel length modulation in NMOS transistors?**

   One of several short-channel effects in MOSFET scaling, channel length modulation (CLM) is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance

2. **Define propagation delay of a CMOS inverter?**

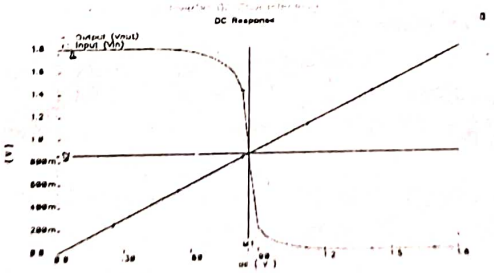
   Propagation delays t_{PLH} and t_{PHL} are defined as the times required for output voltage to reach the middle between the low and high logic levels, i.e. 50 % of VDD in our case of CMOS logic. Figure 1a illustrates the definition of the propagation delays.

3. **Compare CMOS and BiCMOS technology?**

   BiCMOS technology is a combination of Bipolar and CMOS technology. CMOS technology offers less power dissipation, smaller noise margins, and higher packing density. Bipolar technology, on the other hand, ensures high switching and I/O speed and good noise performance.

4. **Draw the DC transfer characteristics of CMOS inverter?**

   A complementary CMOS inverter consists of a p-type and an n-type device connected in series. The DC transfer characteristics of the inverter are a function of the output voltage (Vout) with respect to the input voltage (Vin).



5. **State channel-length modulation. Write down the equation for describing the channel length modulation effect in NMOS transistors?**

   One of several short-channel effects in MOSFET scaling, channel length modulation (CLM) is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

6. **What is Latch-up? How to prevent latch up?**

Latch is the generation of a low-impedance path in CMOS chips between the power supply and the ground rails due to interaction of parasitic pnp and npn bipolar transistors.

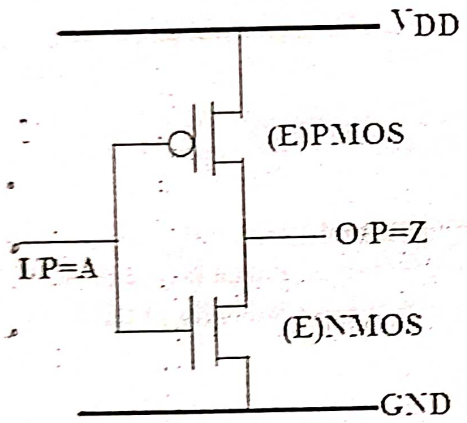
Preventing Latch up

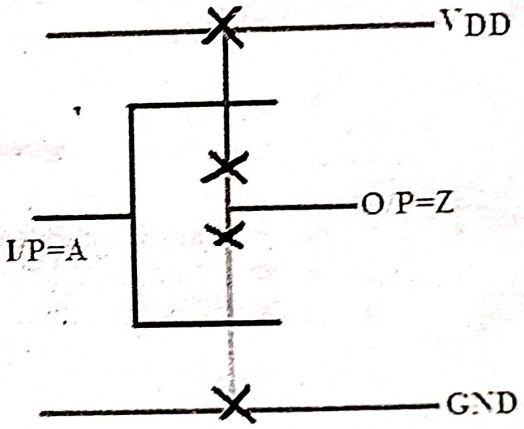
Avoid forward biasing of the source/drain junctions so as not to inject high currents, this solution calls for the use of slightly doped epitaxial layer on top of the heanily doped substrate and has the effect of shunting the lateral currents from the vertical transistor through the low resistance substrate.

7. **Define body bias effect?**

The threshold volatge V_T is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

8. **Draw the stick diagram and layout for CMOS inverter?**





9. **What are the Non ideal IV effects?**

The secondary effects in Mosfet is called non-ideal effects. Some of the non-ideal effects are Velocity saturation, mobility degradation, channel length modulation, subthreshold conduction, body effect, etc.

10. **Discuss any two layout rules?**

1. Scalable Design Rules (e.g. SCMOS, λ-based design rules)
2. Absolute Design Rules (e.g. μ-based design rules)

Unit - 2
Two marks

1) **Define Elmore constant?**

The Elmore delay model explains the delay from input to output of the input signal, which is of a step function type. If the step response of the RC circuit is h(t), 50% point delay of the monotonic step response

2) **State the advantages of transmission gates?**

A transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1.

3) **Define power dissipation?**

The process in which an electric or electronic device produces heat (other waste energy) as an unwanted byproduct of its primary action. Central processing unit power dissipation is a central concern in CMOS architecture.

4) **Define scaling? Mention the types of scaling?**

Two types of scaling are common:

(i) constant field scaling and

(ii) constant voltage scaling.

Constant field scaling yields the largest reduction in the power-delay product of a single transistor. However, it requires a reduction in the power supply voltage as one decreases the minimum feature size.

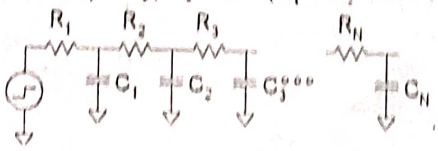
Constant voltage scaling does not have this problem and is therefore the preferred scaling method since it provides voltage compatibility with older circuit technologies. The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages.

5) **Give Elmore delay expression for propagation delay of an inverter?**

The Elmore delay model [Elmore48] estimates the delay from a source switching to one of the leaf nodes changing as the sum over each node i of the capacitance Cion the node, multiplied by the effective resistance Rison the shared path from the source to the node and the leaf.

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i\text{-to-source}} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$



6) **Why single phase dynamic logic structure cannot be cascaded? Justify?**

In dynamic logic, a problem arises when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error.

7) **List out the sources of static and dynamic power consumption?**

Static power is power consumed while there is no circuit activity. For example, the power consumed by a D flip-flop when neither the clock nor the D input have active inputs (i.e., all inputs are "static" because they are at fixed dc levels).

Dynamic power is power consumed while the inputs are active. When inputs have ac activity, capacitances are charging and discharging and the power increases as a result. The dynamic power includes both the ac component as well as the static component.

8) **Define transistor sizing problem?**

It is known that the mobility of holes is approximately 2.5 times lower than that of electrons in Silicon. This property leads to the sizing problems in mosfer which need careful optimization techniques.

9) **Define Dynamic CMOS logic.**

Dynamic logic is distinguished from so-called static logic in that dynamic logic uses a clock signal in its implementation of combinational logic circuits. The usual use of a clock signal is to synchronize transitions in sequential logic circuits. For most implementations of combinational logic, a clock signal is not even needed.

10) **What are synchronizers?**

A synchronizer is a circuit that accepts an input that can change at arbitrary times and produces an output aligned to the synchronizer's clock. Because the input can change dur- ing the synchronizer's aperture, the synchronizer has a nonzero probability of producing a metastable output

Unit – 3
Two marks

1) **What is meant by pipelining?**

A technique used in advanced microprocessors where the microprocessor begins executing a second instruction before the first has been completed. That is, several instructions are in the pipeline simultaneously, each at a different processing stage.

2) **Compare and contrast synchronous design and asynchronous design?**

Synchronous circuits require all elements to exhibit bounded response time. Thus, there is some chance that mutual exclusion circuits will fail in a synchronous system. Asynchronous circuits are more difficult to design in an ad hoc fashion than synchronous circuits.

3) **Implement a 2:1 Multiplexer using pass transistor?**

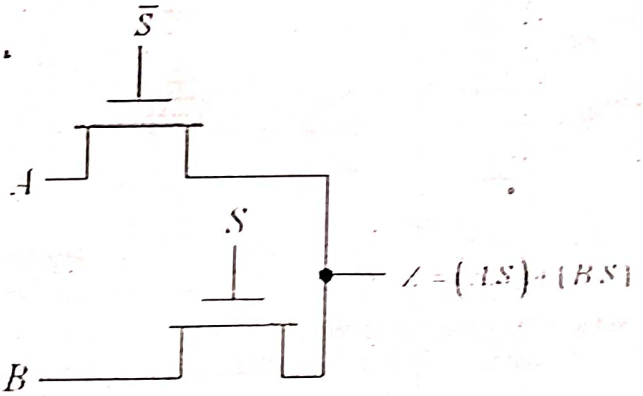
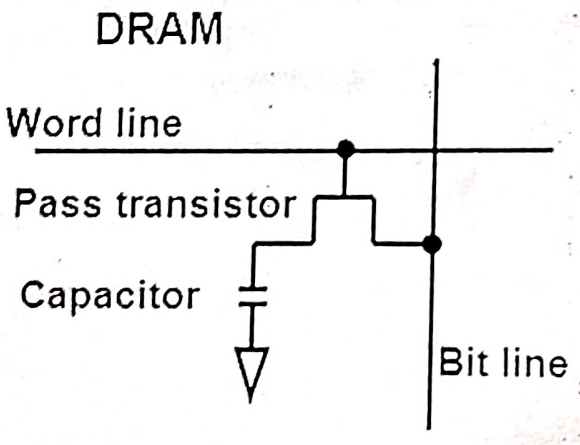
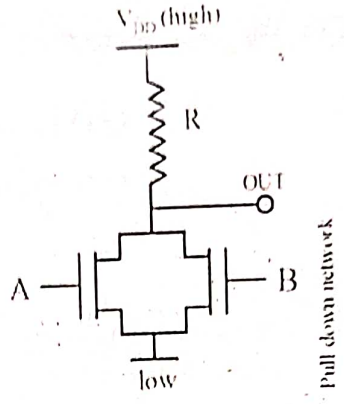


Fig 3 Design of a 2:1 MUX using pass-transistor logic

4) **Design a 1-bit dynamic register using pass transistor?**



5) **Draw the switch level schematic of multiplexer based nMOS latch using nMOS only pass transistors for multiplexes?**



6) **What is clocked CMOS register?**

In the combinational logic, the same clock is used to actually realize combinational logic even NAND and NOR for example. It is generally used to reduce the number of transistors in combinational circuits.

7) **Draw the schematic of dynamic edge-triggered register?**

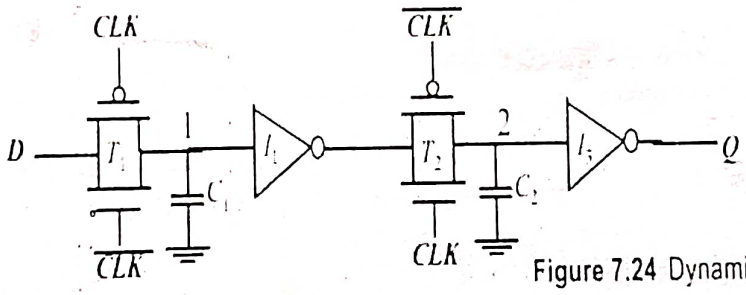


Figure 7.24 Dynamic edge-triggered register.

8) **What are synchronizers?**

A synchronizer is a circuit that accepts an input that can change at arbitrary times and produces an output aligned to the synchronizer's clock. Because the input can change during the synchronizer's aperture, the synchronizer has a nonzero probability of producing a metastable output

9) **State any two criteria for low power logic design?**

Clock disabling, power-down of selected logic blocks, adiabatic computing, software redesign to lower power dissipation are the other techniques commonly used for low power design.

UNIT-IV

1.What are the advantages of data path operators?

To implement the logic function using n-identical circuits.

Data may be arranged to flow in one direction, while any control signals are introduced in an orthogonal direction to the data flow.

2.Define ripple carry adder.

When multiple full adders are used with the carry ins and carry outs chained ogether then this is called a ripple carry adder.

3.What are the different types of high speed adder?

Carry skip addition.
Carry select adder
Carry save ader

4.What are the different types if multipliers available?

Array multiplier
Booth multiplier
Wallace tree multiplier

5.Define booth encoding.

Pipelining reduces cycle time but doesn't reduce the total time required for multiplication.to speed up the multiplying process booth encoding is used. Booth's algorithm takes advantage of the fact that an adder-subtractor is nearly as fast and small as asimple adder.

6.What is meant by Wallace tree multiplier?

Optimized column adder tree
Combines allpartialproducts into 2 vectors
Carry and sum outputs combined using a conventional adder
Delay is log(n)
Irregular routing.

7. What is array multiplier?

Each product terms are the implemented using an array structure of AND and OR gate hence it is called array multiplier.

8.What is meant by barrel shifter?

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle. It can be implemented as a sequence of multiplexers (mux.), and in such an implementation the output of one mux is connected to the input of the next mux in a way that depends on the shift distance.

9. Define accumulator

An accumulator is a register in which intermediate arithmetic and logic results are stored.Without a register like an accumulator, it would be necessary to write the result of each calculation (addition, multiplication, shift, etc.) Tomain memory, perhaps only to be read right back again for use in the next operation.

UNIT-V

1.What is a FPGA?

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

2.What are the types of gate arrays in ASIC?

Channeled gate arrays
Channel less gate arrays
Structured gate arrays

3.What is the full custom ASIC design?

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

4.What is the standard cell-based ASIC design?

A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells. The standard cell areas also called fle4xible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

5. Differentiate between channeled & channel less gate array.

Channeled Gate Array	Channel less Gate Array
1. Only the intereconneet is customized	Only the top few mask layers are customized.
2. The intereconneet uses predefined spaces between rows of base cells.	No predefined areas are set aside for routing between cells.
3. Routing is done using the spaces	Routing is done using the area of transistors unused.
4. Logic density is less	Logic density is higher.

6.Give the constituent of I/O cell in 22V10. 2V10

I/O cell consists of a register an output, a 4:1 mux, tristate buffer and 2:1 input mux. It has the following characteristics:

* 12 inputs
* 10 I/Os
* product time 9 10 12 14 16 14 12 10 8
* 24 pins

7. Give the different types of ASIC.

Full custom ASICs

Semi-custom ASICs

- standard cell based ASICs
- gate-array based ASICs

Programmable ASICs

- Programmable Logic Device (PLD)
- Field Programmable Gate Array (FPGA).

8. What are the different methods of programming of PALs?

The programming of PALs is done in three main ways:

- Fusible links
- UV – erasable EPROM
- EEPROM (E PROM) – Electrically Erasable Programmable ROM

9. Give the steps inASIC design flow.

Design entry
Logic synthesisSystem partitioning
Prelayout simulation.
Floorplanning
Placement
Routing
Extraction